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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,881	01/18/2000	Kie Y Ahn	303.672US1	8976
21186	7590	02/14/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			NGUYEN, HA T	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/483,881

Applicant(s)

AHN ET AL.

Examiner

Ha T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3,5,7-42 and 65 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3,5,7-42 and 65 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule-17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12-27-4</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Notice to applicant

1. Applicants' Amendment and Response to the Office Action mailed Oct. 9, 2005 has been entered and made of record.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(a) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 8-10 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tan et al. (USPN 6372622, hereinafter "Tan") in view of Matsuda et al. (USPN 6403481, hereinafter "Matsuda").

Referring to Figs. 2-6 and related text, Tan discloses [Re claims 8-9] a method for forming copper vias on a substrate, comprising: depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a semiconductor substrate 10 using a sputtering deposition technique (see col. 3, lines 30-53); depositing a patterned photoresist over the seed layer, wherein depositing a patterned photoresist defines a first number of via holes above the seed layer (see Fig. 2); and depositing a layer of copper over the seed layer (see par. bridging cols. 3

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and 4). But it does not disclose expressly using electroless plating to form the copper layer, the thickness and the discontinuity of the seed layer. However, the missing limitations are well known in the art because Matsuda discloses the use of Cu electroless plating on discontinuous seed layer and the thickness of seed layer (see Figs. 1-7B, Summary, col. 5, lines 48-55, and col. 6, line 55- col. 7, line 52).

[Re claim 10] Tan also discloses forming a number of copper vias, wherein the copper vias are formed on the seed layer but not on the patterned photoresist layer (see Fig. 3).

[Re claims 34-37] The combined teaching of Tan and Matsuda discloses substantially the limitations of claims 34-37. But it does not disclose the repetition of steps to form up to a second level of copper lines. However, the transposition of process steps or the splitting of one steps into two, where the processes are substantially identical or equivalent in terms of function, manner and result was held not to patentably distinguish the processes (Ex Parte Rubin, 128 USPQ 440 (Board of Appeals 1959)).

Therefore, it would have been obvious to combine Tan and Matsuda to obtain the invention as specified in claims 8-10 and 34-37.

4. Claims 3, 5, 7, 12, 38-42, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tan in view of Matsuda and Naik et al. (USPN 6245662, hereinafter "Naik").

Referring to Figs. 2-6 and related text, Tan discloses [Re claims 7, 12, 38, 39, and 65] a method for forming copper vias on a substrate, comprising: depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a semiconductor substrate 10 (see col. 3, lines 30-53); using a photolithography technique in order to define a first number of via holes above the seed layer (see Fig. 2); and depositing a layer of copper over the seed layer (see par. bridging cols. 3 and 4); and removing the photoresist layer (see col. 5, lines 1-5). But it does not disclose expressly using electroless plating to form the copper layer, the thickness and the discontinuity of the seed layer; and removing the photoresist layer using oxygen plasma ashing. However, the missing limitations are well known in the art because Matsuda discloses the use of Cu electroless plating on discontinuous seed layer and the thickness of seed layer (see Figs. 1-7B, Summary and col. 6, line 55- col. 7, line 52) and Naik discloses that oxygen plasma ashing of the photoresist is conventionally done, this etching also cause removal of exposed copper (see

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col. 6, lines 28-36). A person of ordinary skill is motivated to modify Tan with Matsuda and Naik to use electroless plating to deposit Cu to obtain good electromigration resistance (see Matsuda, col. 2, lines 11-22) and oxygen plasma ashing photoresist and Cu seed layer.

[Re claim 3] Tan also discloses wherein depositing a seed layer includes depositing a seed layer using a physical vapor deposition process (see col. 3, lines 40-53).

[Re claim 5] Tan does not disclose expressly wherein depositing a layer of copper includes filling the number of via holes to a top surface of the photoresist layer. However, Tan discloses Cu can be filled to be totally within the openings or overlapping the edges of the photoresist (col. 4, lines 1-8), this implies that the height of Cu in the openings formed in the photoresist varies with the need of a specification, including the height to a top surface of the first patterned photoresist layer when a stud having a height equal to the thickness of the photoresist is needed in the application (see Fig. 3).

[Re claims 40-42] Tan discloses the use of a diffusion barrier layer under a copper contact (see col. 3, lines 40-53). When repeating the steps of forming contacts (vias or wiring lines), the barrier layer of the subsequent level (vias or wiring lines) is formed on the previously formed level. But it does not disclose the use of a diffusion barrier on the second level of copper lines and the claimed material. However, the examiner takes Official Notice that, these features are well known in the art, they are intended to effectively prevent Cu diffusion to the surrounding environment

Therefore, it would have been obvious to combine Tan with Naik and Matsuda to obtain the invention as specified in claims 3, 5, 7, 12, 38-42, and 65.

5. Claims 5, 11, and 13-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tan in view of Matsuda or Tan in view of Matsuda and Naik and Andricacos et al. (USPN 5937320, hereinafter "Andricacos").

[Re claims 5, 11, 13-15, 17] The combined teaching of Tan and Matsuda or Tan, Matsuda and Naik discloses substantially the limitations of claims 5, 11, and 13-14, as shown above. It also discloses the forming of a second patterned photoresist defining a number of line openings above the copper vias (see Figs. 7A-B). But it does not disclose expressly the repetition of the steps in the forming of the vias to form conductive lines and filling Cu to a top

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surface of the first patterned photoresist layer. However, Tan discloses Cu can be filled to be totally within the openings or overlapping the edges of the photoresist (col. 4, lines 1-8), this implies that the height of Cu in the openings formed in the photoresist varies with the need of a specification, including the height to a top surface of the first patterned photoresist layer when a stud having a height equal to the thickness of the photoresist is needed in the application (also see Andricacos, Fig. 3 (e) for the teaching of this feature); besides, the transposition of process steps or the splitting of one steps into two, where the processes are substantially identical or equivalent in terms of function, manner and result was held not to patentably distinguish the processes (Ex Parte Rubin, 128 USPQ 440 (Board of Appeals 1959). Besides, depositing a seed layer by evaporation is conventionally done in the art.

[Re claim 16] Tan also discloses forming a number of copper vias, wherein the copper vias are formed on the seed layer but not on the patterned photoresist layer (see Fig. 3].

[Re claim 18] The combined teaching of Tan, Andricacos and Matsuda discloses substantially the limitations of claim 18. But it does not disclose that the thickness of the second patterned photoresist is less than that a thickness of the first patterned photoresist layer. However, it is within the level of skill of a person of ordinary skill in the art to deposit the second patterned photoresist layer to a thickness suitable for a specific application, including less than a thickness of the first patterned photoresist layer.

[Re claim 19] Tan discloses wherein depositing the second patterned photoresist layer which defines a second number of line openings includes a number of first level line openings (see Fig. 4).

[Re claims 20 and 21] The combined teaching of Tan, Matsuda, and Andricacos discloses substantially the limitations of claims 20 and 21, as shown above. But it does not disclose expressly forming second and third seed layers, second and third patterned photoresist layer, first level of conductor lines, the second level copper vias. However, the argument concerning the repetition of steps used for the rejection of claim 13 also applies.

[Re claims 22-27] The argument used for the rejection of claims 7, 13, 14, 16, and 18 concerning the respective claimed features apply.

[Re claims 28-30] The combined Tan, Matsuda, and Andricacos discloses substantially the limitations of claim 28, as shown above. But it does not disclose removing photoresist layers

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by oxygen plasma ashing which also removes seed layers. However, these features are well known in the art, because Naik discloses these features (see col. 6, lines 28-36). Besides, depositing a seed layer by evaporation is conventionally done in the art.

[Re claims 31-33] Matsuda discloses wherein depositing seed layer having discontinuous island structure by sputtering to a thickness of less than 15 nm (see Fig. 1, #13, col. 5, lines 39-55).

6. Claims 13-42 are rejected as being unpatentable over the combination of Tan, Matsuda and/ or Naik and/or Andricacos in view of Simpson (USPN 6197688)

The combination of Tan, Matsuda and/ or Naik and/or Andricacos discloses substantially the limitations of claims 13-42, as shown above. It also discloses the forming of a second patterned photoresist defining a number of line openings above the copper vias. But it does not disclose expressly the repetition of the steps in the forming of the vias to form conductive lines. However, the missing limitation is well known in the art because Simpson discloses that separately forming conductive vias then repeating the steps to form conductive lines are conventional in the art (See fig. 9).

Therefore, it would have been obvious to combine Tan and Matsuda with Simpson to obtain the invention as specified in claims 13-42.

Response to Applicants' arguments

7. Applicants' arguments with regard to the rejections under 35 U.S.C. 103 have been fully considered, but they are not deemed to be persuasive for at least the following reasons.

Applicants argued mainly that the combined teaching of Tan with Matsuda does not teach the step of electroless plating a metal (Cu) on a discontinuous seed layer. More specifically, applicants argued that Matsuda does not teach the use of a discontinuous seed layer for electroless plating a metal (Cu). After a very careful review of Matsuda, the examiner still disagreed. Tan clearly discloses a seed layer of Cu sputtered over a barrier layer 14 which is itself formed on a semiconductor substrate 10 (see col. 3, lines 30-53 specifically lines 43-46). Tan does not disclose the details about the seed layer. In the first example of the first embodiment (Figs. 1-3), Matsuda discloses electroless plating Cu layer 14 on island like

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discontinuous seed layer 13. In the third example of the first embodiment (Figs. 7A-7B), Matsuda also discloses electroplating or electroless plating Cu layer 57 on a sputtered discontinuous Cu seed layer 56, as clearly shown in Figs. 7A-7B. Matsuda discloses that Cu layer 57 can be formed by either electroless plating or electroplating (see col. 7, lines 8-14). At least from the three examples given for the first embodiment, it is shown that there are advantages to use electroless plating process compared to electroplating. In the second example of the first embodiment (Figs. 4-6), Matsuda shows clearly that when electroplating is used, current has to be applied and a conductive layer 32 has to be formed to supply current for the electroplating. Even when the affects of the current supplied on the film electroplated are not considered, the requirements for the application of a current and the formation of a conductive layer to supply the electroplating current are additional expenses that would make electroless plating more attractive than the more costly electroplating process.

Therefore, the combinations of Tan with the applied references do disclose all the limitations of the rejected claims 3, 5, 7-42 and 65 and there is a good motivation to combine Matsuda with Tan, lowering manufacturing cost.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

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9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha T. Nguyen whose telephone number is (571) 272-1678. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The telephone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ha Nguyen
Primary Examiner
2- 8 - 05